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The role of the CdS buffer layer in $CuGaSe_2$-based solar cells

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Abstract

We present some results for Ga-rich $CuGaSe_2$-based solar cells using different conditions for deposition of the CdS buffer layer. Three different recipes for the growth of the CdS buffer layers at 60 and 80 °C are compared. This work shows the importance of the adaptation of the CdS growth to the absorber layer. A maximum open circuit voltage V_{oc} of 922 mV is achieved by using 60 °C as the chemical bath temperature and lower thiourea and ammonia concentrations. Temperature-dependent current–voltage and room temperature drive-level capacitance profiling measurements are carried out to study the CdS/$CuGaSe_2$ interface properties. All devices are characterized by tunnelling-enhanced interface recombination. However, results show that the higher V_{oc} obtained for the low bath temperature coincides with a reduced tunnelling component. This can be attributed to a lower net doping level in the space charge region. Secondary ion mass spectrometry analysis reveals Cu diffusion into the buffer layer when CdS is made at 80 °C. This agrees with the higher charge density observed for those devices, enhancing the tunnelling.

1. Introduction

There is a considerable interest in the development of solar cells based on wide bandgap absorbers. They promise interesting advantages for module implementation, due to the high voltage and low current output characteristics. Another area of interest, where efforts are focused now, is the development of tandem structures. $CuGaSe_2$ (CGS) with a band gap of 1.7 eV is in principle a good candidate to be used as the top cell in a mechanically stacked tandem structure [1]. Current record solar cells have been prepared from $CuGaSe_2$ single

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crystals and have reached efficiencies of 9.7% with a V_{oc} of 946 mV [2], while a 9.5% efficient record cell with V_{oc} of 905 mV has been prepared from polycrystalline CGS thin films [3]. In our laboratory, an efficiency of 8.7% [4] has been obtained by using a chemical close-spaced vapour transport (CCSVT) technique and of 8.2% by a bilayer process [5] for CGS thin film deposition. However, the efficiencies of CGS-based devices are still behind the values achieved for the lower-gap chalcopyrites [6]. The most crucial drawback of CGS solar cells is the low open circuit voltage V_{oc} compared to the band gap. This situation, however, could be overcome if conduction type inversion at the surface of the absorber is obtained [7]. But this seems to be difficult to achieve with high gap chalcopyrites [8], the p/n junction being located at the CdS/CGS interface. This fact together with the negative offset of the conduction band between the buffer and the absorber layer cause a pronounced dependence of the electrical parameters of the solar cell on the quality of the interface because of interface-related and tunnelling-assisted recombination mechanisms. Therefore, a careful adaptation of the growth of CdS onto CGS is necessary.

Nadenau *et al* [9] have reached open circuit voltages of 940 mV, but the losses in the fill factor (FF) and short circuit current density (J_{sc}) resulted in efficiencies in the range of 5.0% for polycrystalline solar cells. A similar behaviour has been observed by Nishiwaki *et al* [10] with a V_{oc} of 908 mV and an efficiency of 4.3%. More recently, Young *et al* [3] achieved the maximum V_{oc} to date of 971 mV for $CuGaSe_2$ polycrystalline solar cells; this was obtained after 2 min annealing in air.

In this work, we study solar cells based on Ga-rich $CuGaSe_2$ prepared by the three-stage co-evaporation process. Once the absorber preparation conditions have been optimized, different recipes for the CdS layer deposition are used in order to increase the open circuit voltage without reducing the efficiency of the solar cells. The elemental distribution at the CdS/CGS interface in conjunction with the electrical properties of different solar cells are investigated to clarify the influence of the buffer layer on the device parameters.

2. Experimental details

2.1. Absorber and solar cell preparation

CGS thin films are grown on Mo coated soda-lime glass (SLG) using co-evaporation in a three-stage process, as described elsewhere [11]. Laser light scattering (LLS) together with a pyrometer are used as an *in situ* process control, which has proven to be extremely valuable [12, 13]. For LLS the light source is a 635 nm red laser and the detector is a photomultiplier with lock-in technology. Heat radiation from the sample was monitored by the pyrometer placed with its line of view perpendicular to the substrate surface. The nominal substrate temperature is measured by a thermocouple behind the substrate. The temperatures are given as measured in the experimental set-up and hence depend on several parameters such as, for example, the position of the thermocouple. Figure 1 illustrates the three-stage process together with typical results for LLS and the pyrometer profiles for a CGS process on Mo/glass. Once the first stoichiometric point s_1 is passed, i.e. [Cu]/[Ga] > 1, the scattered laser light intensity increases significantly because of the higher roughness of the Cu-rich film. Past stoichiometry s_1, the film temperature decreases with time during the addition of Cu, as can be seen from the pyrometer signal. This is due to a higher emissivity of Cu–Se phases compared to that of stoichiometric CGS or Ga-rich CGS films [14].

Solar cells with a Ni–Al/ZnO/CdS/CGS/Mo/soda-lime glass structure have been fabricated. The treatment of the absorber surface and the deposition method of the CdS layer are crucial for the device performance. The CdS is deposited by chemical bath deposition (CBD). The standard bath temperature for CdS layer deposition for applications

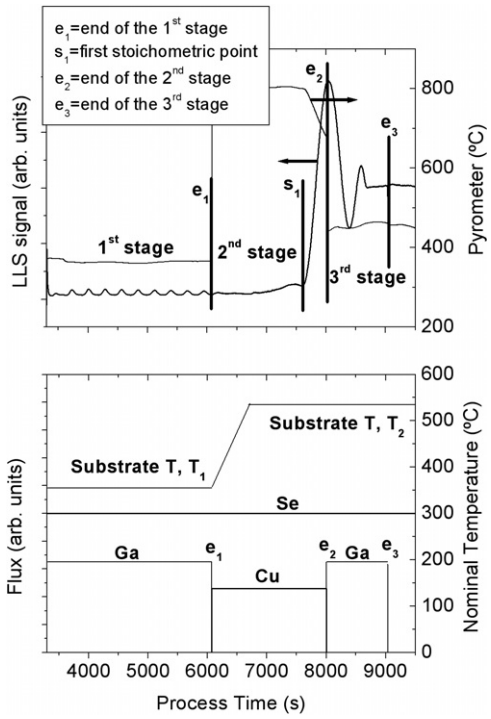

Figure 1. Pyrometer and LLS signal transients and the flux schematics for a three-stage $CuGaSe_2$ process on Mo/SLG.

Table 1. Comparison of the deposition conditions for CdS layers.

Recipe	T (°C)	Cd salt, concentration (mM)	S^{2-} source, concentration (M)	Additive NH_3 (M)	Time (min)
1	60	1.30	0.11	1.0	8
2	80	1.24	0.22	1.5	6
3	80	1.30	0.11	1.0	6

on $CuInSe_2$ and $Cu(In, Ga)Se_2$ with low Ga content is 60 °C. Some authors have used elevated bath temperatures at 80 °C, showing an enhanced performance of the $CuGaSe_2$-based solar cells [15]. Table 1 compares the different recipes for the CdS layer deposition used in this work. Recipe 1, at 60 °C, is the same as the one used in our laboratory for the preparation of $Cu(In, Ga)Se_2$ solar cells [13]. A second recipe, recipe 2, is introduced because of the most recent research and optimization of the CdS layer for $CuGaSe_2$, carried out in our lab [16]. In contrast to this work, in [16] $CuGaSe_2$ was deposited by a bilayer process [5]. We have already reported that the properties of the absorber using the bilayer process are different from those obtained by a three-stage process (see some details in the first paragraph on section 3) [17]. Recipe 3 is introduced in order to compare the effect of the bath temperature. The sputtered window layer consists of a double ZnO layer: a thin intrinsic layer and a highly conductive Al-doped ZnO layer. Ni/Al grids are evaporated by e-beam to facilitate current collection.

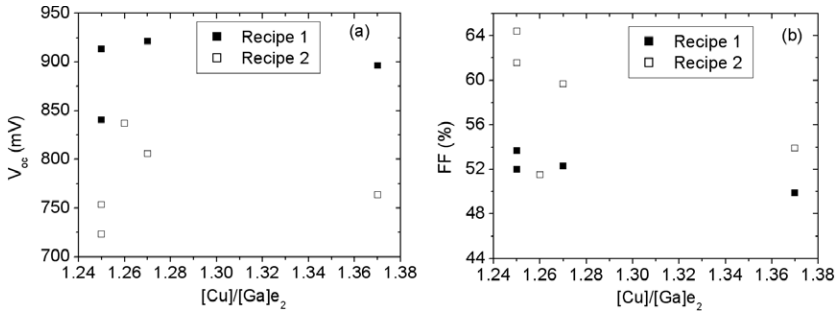

Figure 2. (a) V_{oc} and (b) FF versus the atomic ratio [Cu]/[Ga]e$_2$ at the end of the second stage of the three-stage process for different devices using recipes 1 and 2 for CdS layer deposition.

2.2. Characterization techniques

The absorber composition and thickness determination of the CGS films are found by means of x-ray fluorescence analysis (XRF) using a Philips MagiXPro PW2400 spectrometer. The final composition of these absorbers is Ga rich with an atomic ratio [Cu]/[Ga]e$_3$ between 0.89 and 0.92 and a thickness between 1.9 and 2.5 μm.

Secondary ion mass spectrometry (SIMS) experiments are conducted using a SAJW-05 instrument, in which the mass spectrometer is a Balzers QMA-410 quadrupole-based one. The apparatus is also equipped with physical electronics ion gun with an Ar^+ beam of about 100 μm in diameter. In order to reduce atomic mixing during sputtering and thus increase the depth resolution [18] an ultra-low energy primary beam of 880 eV was applied in depth profiling of the CdS/CGS interfaces.

The photovoltaic (PV) parameters are determined from J–V measurements carried out under AM1.5 illumination, 100 mW cm^{-2} intensity, at 25 °C. The total area of the solar cell devices is 0.5 cm^2. The external quantum efficiency (EQE) is measured with a two-source illumination system (xenon and halogen lamp), a monochromator (Bentham TM300) and a calibrated Si diode as reference. The UV/VIS/NIR reflection spectra of CGS solar cells are recorded using an integrating sphere. The internal quantum efficiency is calculated from the EQE and the reflectance measurements of the solar cell.

Measurements of the current–voltage characteristics as a function of temperature (JV–T) and illumination are performed in an evacuated N_2-cooled cryostat using a Keithley source measurement unit in four-point configuration. The samples are illuminated by a halogen lamp. A set of neutral density filters serves to adjust the light intensity.

Drive-level capacitance profiling is performed at room temperature and $f = 40$ kHz using an HP4284 impedance analyser.

3. Results and discussion

As has previously been reported [17], the efficiency of the device depends on the absorber morphology, which is strongly influenced by the Cu content during the growth process. The three-stage process is characterized by a possible broader Cu-excess window at the end of the second stage. The decreased FF at extremely Cu-rich composition after the second stage is related to the voids observed in the structure of the absorber [17]. In figure 2, the variation of V_{oc} and FF with the composition at the end of the second stage, [Cu]/[Ga]e$_2$, is shown for solar cells using the CdS recipes 1 and 2. It is observed that the highest V_{oc} corresponds to a [Cu]/[Ga]e$_2$

Table 2. PV parameters of solar cells with the different CdS deposition conditions.

Batch	$[Cu]/[Ga]_{e2}$	T_2 (°C)	Recipe CdS	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF (%)	η (%)
A2318	1.27	540	1	922	14.5	52.3	7.0
			1 after 10 months	805	16.0	61.4	7.9
			2	806	12.3	45.6	4.5
			2 after 10 months	793	12.6	55.5	5.6
A2334	1.25	540	1	914	14.7	52.0	7.0
			2	723	14.4	61.6	6.4
A2349	1.25	535	1	841	14.7	53.7	6.6
			2	754	14.5	64.4	7.0
			3	808	14.4	56.4	6.6
A2428	1.27	540	2	761	16.4	57.1	7.1
			3	859	14.5	57.8	7.2

atomic ratio of 1.26–1.27 after the second stage, in particular for recipe 2, coinciding with a larger grain formation [17]. Independently of the CGS thin film composition, a clear tendency of V_{oc} and FF related to the type of CdS buffer layer deposition recipe is observed. The open circuit voltage of the devices whose CdS layer was deposited by recipe 1 ($T_{CBD} = 60\,°C$) is much higher than for devices made with recipe 2. The opposite behaviour is obtained for the FF. An open circuit voltage of 922 mV has been produced using the lower chemical bath temperature. However, the low FF prevents improved device efficiencies. Analysis of I–V curves using a one-diode model shows that the diode quality factor A and the saturation current density J_0 of the devices are lower when using recipe 1 for the CdS layer deposition. This could explain the higher V_{oc} for these devices. On the other hand, the series resistance R_s of the devices using recipe 2 is generally lower, yielding a better FF.

The PV parameters of different CGS solar cells with the different CdS layer deposition conditions are shown in table 2. Four representative absorber batches are presented with a final composition of $[Cu]/[Ga]e_3$ around 0.9. T_2 is the nominal substrate temperature at the second and third stage of the co-evaporation process. As can be seen, the short circuit current is almost constant or slightly higher for the lower chemical bath temperature, in contrast to other works [15, 19]. We should take into account that recipes 1 and 2 differ not only in the bath temperature but also in the concentration of the Cd salt and of the sulfur source (thiourea). This shows the importance of the concentration of the constituents within the chemical bath and the need to optimize the buffer layer for the particular $CuGaSe_2$. In order to compare only the effect of the bath temperature on the PV parameters of the device, another recipe is introduced, recipe 3. This recipe uses the same concentration of bath constituents as recipe 1, but the temperature is increased to 80 °C. Compared to recipe 1, the solar cells using recipe 3 for the CdS layer are characterized by a decreased V_{oc} and a slightly increased FF, without leading to a significant increase in the efficiency. The remaining main difference between recipe 2 and the others is the thiourea and ammonia concentrations. Results from table 2 show that the lower thiourea and ammonia concentrations (recipes 1 and 3) produce higher V_{oc}.

The p/n junction is located near the interface between the $CuGaSe_2$ and CdS layers. This emphasizes the importance of interfacial interactions between the two layers. Figure 3 shows SIMS depth profiles of the CdS/CGS interface formed with the same absorber and different CdS deposition conditions. The depth profiles of sputtered Ga^+, Se^+, S^+, Cd^+ and also Cu^+/Na^+ ratios are plotted against sputter time. The copper distribution in the investigated interfaces is represented by the ratio of Cu^+/Na^+, since anomalous behaviour of the Cu signal was noticed

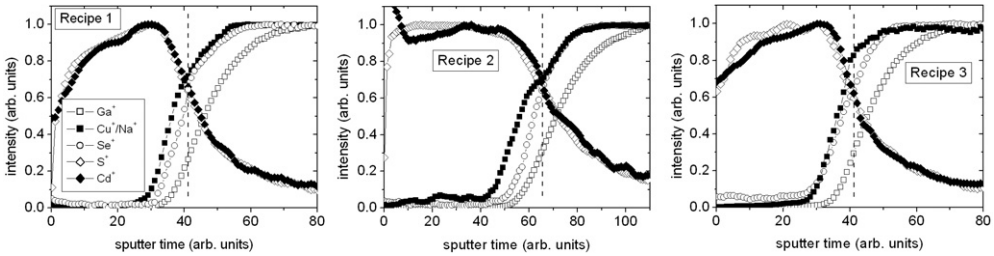

Figure 3. SIMS depth profiles taken with 880 eV Ar^+ beam of the CdS/$CuGaSe_2$ interfaces based on the same absorber batch and different CdS deposition conditions. The data have been normalized to the maximum value of ion intensity of sputtered secondary ions. The dashed lines indicate the position of the interface.

(characteristic maximum at the interfaces) caused by the presence of sodium. This feature might be associated either with matrix effects caused by the presence of Na at the interfaces (which increases Cu^+ emission) or with ion mass interferences containing Na (e.g. $NaAr^+$ has the same mass as $^{63}Cu^+$, where Ar is the beam element; however, also in profiling measurement of the interfaces the same feature represents the isotope $^{65}Cu^+$). The profiles depicted in figure 3 do not reveal much difference between the first two recipes. It seems that only a slightly stronger in-diffusion of Cu into the CdS buffer layer takes place for recipe 2. Whereas $CuGaSe_2$-based thin film solar cells using recipe 1 for the CdS layer deposition present V_{oc} up to 922 mV, a V_{oc} no higher than 840 mV is achieved when using recipe 2. The higher Cu diffusion into the buffer layer for the higher bath temperature would create Cu vacancy sites V_{Cu}^-, increasing the doping level of the absorber surface. This could decrease the V_{oc} due to a higher recombination with a smaller width of the space charge region. For Cu-rich absorbers, Nadenau *et al* [15] have also observed a much stronger interaction between Cu and the buffer layer for a bath temperature of 80 °C. The large difference in the behaviour of Cu showed that the interaction is not related to a diffusion process but to a chemical reaction between the surface of the absorber layer and the solution used for the deposition of CdS. In order to clarify the possible reason for the lower V_{oc} with a higher chemical bath temperature, JV–T, drive level capacitance profiling (DLCP) and EQE measurements were carried out.

The conduction band offset at the CdS/absorber interface alters from a spike, which is the situation for a low Ga-content $CuIn_{1-x}Ga_xSe_2$, to a cliff for $CuGaSe_2$ [20]. The missing inverted surface for $CuGaSe_2$ and the development of a barrier suggest the model of a junction-dominated recombination process. For the investigation of the transport mechanism in ZnO/CdS/$CuGaSe_2$, solar cell devices with CdS grown using recipes 1–3 were chosen. The dark JV–T curves were studied following the model proposed for the chalcopyrite solar cells [21]. The forward current density J of the heterojunction is described by

$$J = J_0 \exp\left(\frac{qV}{AkT}\right) = J_{00} \exp\left(\frac{-E_a}{AkT}\right) \exp\left(\frac{qV}{AkT}\right) \tag{1}$$

where kT/q is the thermal voltage, J_{00} is a weakly temperature-dependent prefactor and E_a is the activation energy of recombination. By reorganizing equation (1) to the relationship

$$A \ln(J_0) = -\frac{E_a}{kT} + A \ln(J_{00}) \tag{2}$$

a refined evaluation of E_a is attained, in the case where A does not overly depend on temperature itself. Thus, a plot of $A \ln(J_0)$ versus the inverse temperature $1/T$ should yield a straight line with a slope corresponding to the activation energy E_a. The temperature

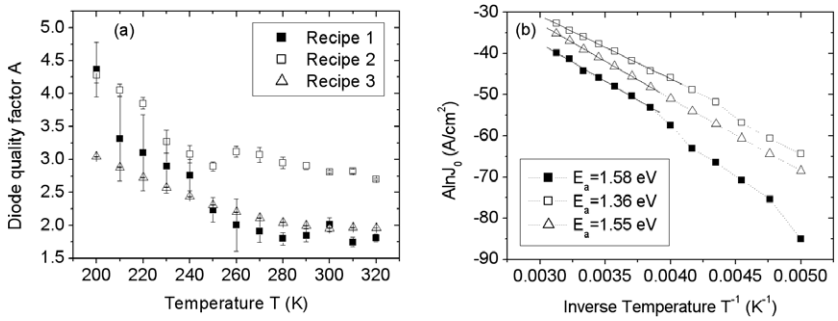

Figure 4. (a) Temperature dependence of the diode quality factors and (b) modified Arrhenius plot of the saturation current density corrected by the diode quality factors A of the devices using recipes 1–3 for the CdS layer deposition.

dependence of the diode quality factors A in the dark is given in figure 4(a). A diode factor $A > 2$ indicates a strong contribution of tunnelling to the recombination current. The diode quality factor A is less than 2 at higher temperatures and increases above 2 for temperatures below 260 K when recipe 1 is used for the chemical bath deposition. However, the diode factor is always higher than 2 when recipe 2 is used. The devices using recipe 3 as the CdS deposition condition present a more similar behaviour to that observed for recipe 1. So, the diode factor A is at around 2 at higher temperatures and increases above 2 below 290 K. Whereas the tunnelling contribution dominates the recombination process in the whole temperature range when using recipe 2, it only happens at temperatures below 260 K and below 290 K for recipes 1 and 3 respectively. Cu diffusion into the buffer layer could create a higher concentration of negatively charged V_{Cu}^{-} within a defective surface layer [22]. Consequently, the high charge density would enhance tunnelling.

The activation energy of the recombination is determined from the modified Arrhenius graphs shown in figure 4(b). The saturation currents are obtained from the analysis of the dark JV characteristic plots and E_{a} is extracted using the area where A is constant. The analysis of the dark measurements gives $E_{\mathrm{a}} = 1.58$, 1.36 and 1.55 eV using recipes 1, 2 and 3, respectively. All of them are below the band gap energy of 1.68 eV. The effective band gap energy is determined from EQE measurements. Therefore, the dominant recombination process takes place at the CdS/CGS interface here. We could conclude that all devices are characterized by tunnelling-enhanced interface recombination, but with a stronger tunnelling component for the device with the CdS from recipe 2. The more significant tunnelling coincides with the lower V_{oc} of the devices and the increased activation energies correlate with the increased V_{oc}.

Drive-level capacitance measurements are used to extract defect and/or carrier densities for the solar cells with the different CdS layer deposition conditions. Standard capacitance profiling has been shown to be quite sensitive to the presence of interface states [23]. Much more reliable results can be obtained from drive-level profiling in which nonlinear terms of the capacitance response are collected by varying the modulation amplitude. Figure 5 displays the DLCP-profiling for different solar cells. The profiles show an increase in the defect density towards the heterointerface. A clear minimum in the profiling density at about 300 nm and at around 470 nm from the interface can be discerned for the devices using recipes 2 and 3, respectively, for the CdS layer deposition. However, the minimum is at a position varying between 500 and 800 nm for the solar cells using recipe 1. On the another hand, $CuGaSe_2$ solar cells made from the buffer layer at 80 °C exhibit a higher doping density. This high total charge density is the reason for larger tunnelling-enhanced recombination losses and the lower V_{oc}.

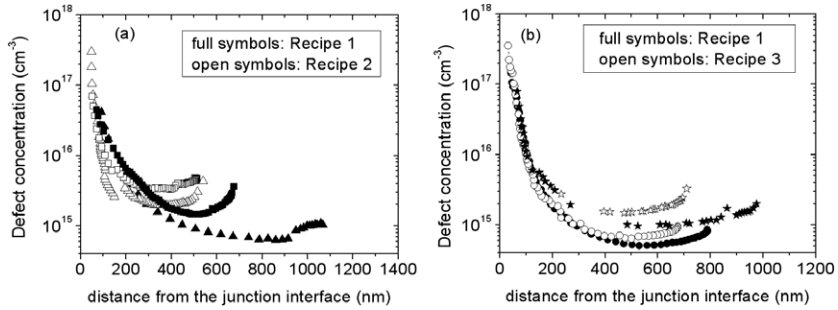

Figure 5. DLCP profiles taken at room temperature for different solar cells. CdS deposition conditions: (a) recipes 1 and 2 and (b) recipes 1 and 3. The same symbol represents the same absorber batch.

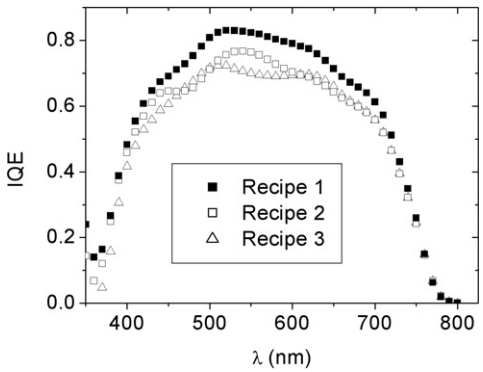

Figure 6. Internal QE of ZnO/CdS/CGS solar cells using the three recipes for CdS layer deposition.

It may be deduced that there is a larger depletion region width connected to the lower carrier density when using recipe 1 for the CdS deposition conditions.

Figure 6 shows the internal quantum efficiency (IQE) for some devices using the three different recipes for the CdS layer deposition. The IQE is superior in the whole range of wavelengths when using recipe 1 for the buffer layer. A lower thiourea concentration should slow down the growth of the CdS layer [24]. The lower CdS deposition rate and the lower bath temperature seem to be favourable for the formation of a better quality of CdS/CGS interface. The increase of the bath temperature to 80 °C increases the CdS growth rate. This makes the CdS/CGS interface properties change in such a way that the IQE decreases across the whole photosensitive region of the device. However, there is no difference in the response near the bandedge for all different CdS deposition conditions. This indicates that it may be reasonable to assume that the bulk material of the absorber is identical in all cases.

Figure 7 shows the band diagram of the ZnO/CdS/$CuGaSe_2$ heterostructure as proposed by Nadenau *et al* [9, 19]. We assume a valence band offset $\Delta E_v = 0.9$ eV determined by Nadenau *et al* by x-ray photoelectron spectroscopy (XPS) at the $CuGaSe_2$/CdS interface [19] and $E_{gCuGaSe_2} = 1.68$ eV determined from our EQE measurements. With these data and a CdS bulk band gap of $E_{gCdS} = 2.42$ eV, we obtain a conduction band offset $\Delta E_c = -0.16$ eV following the expression $\Delta E_c = E_{gCdS} - E_{gCuGaSe_2} - \Delta E_v$. The activation energy of recombination calculated by the expression $E_a = E_{gCuGaSe_2} - \Delta E_c$ is 1.52 eV, corresponding

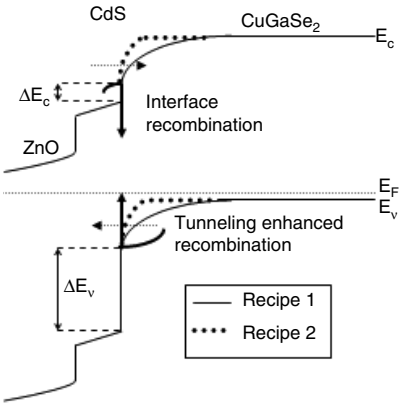

Figure 7. Band diagram of a ZnO/CdS/$CuGaSe_2$ heterostructure with a conduction band offset ΔE_c and a valance band offset ΔE_v between $CuGaSe_2$ and CdS.

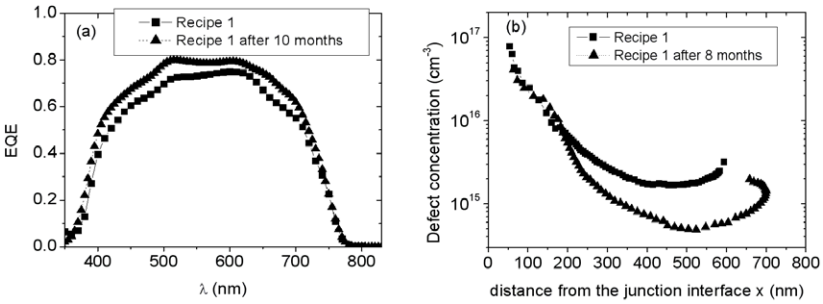

Figure 8. (a) External quantum efficiency curves and (b) DLCP of a CGS solar cell before and after some months in air.

to the maximum barrier $E_{b,max}$ for interface recombination [4]. There is a vague correlation between the calculated recombination energy using the band diagram in figure 7 and the experimentally found value from the JV–T analysis in the dark using recipes 1 and 3 for the CBD CdS. As has been previously mentioned, $E_{gCuGaSe_2}$ is the same for all recipes. The behaviour of the solar cells made using recipe 2 could be represented by dotted lines in the ZnO/CdS/$CuGaSe_2$ band diagram (figure 7).

The solar cells were kept in air for some months. After that, some of them were analysed again. The solar cells were characterized by a decrease in V_{oc} and an increase in J_{sc} and FF, which led to an enhanced efficiency (see table 2). The EQE and the DLCP profiles of a device using recipe 1 as the CdS layer deposition condition are shown in figure 8. The spectral response increases across the entire wavelength interval after storage, producing a higher increased J_{sc}. The band gap of the absorber remains unchanged. However, the electronic properties change, and a lower net doping is observed (see figure 8(b)). Thus, storage seems to change the CdS/$CuGaSe_2$ interface properties. This could be due to diffusion of Cd into absorbers, leading to Cd on Cu sites, Cd^+_{Cu} and removing V^-_{Cu} [25], so that a higher collection current occurs. Another possible reason could be because of the passivation of the absorber grain boundaries (GBs) by the sulfur which diffuses along GBS [26]. This would result in an enhanced J_{sc}, as is observed. This again shows the sensitivity of the interface. Further

investigations are necessary in order to clarify the origin of the enhanced device efficiencies after storage.

4. Conclusions

This work shows the importance of the adaptation of the CdS buffer layer on respective $CuGaSe_2$ absorber films. A maximum V_{oc} of 922 mV has been achieved for CGS solar cells made from the CdS layer using recipe 1, at 60 °C and low thiourea and ammonia concentrations. Several reasons could explain the higher V_{oc} when recipe 1 is used for the chemical bath deposition. DLCP measurements reveal a decrease of the doping concentration. Increased carrier collection is observed by spectral response measurements. All these factors help to reduce the tunnelling probability. Although the dominant recombination process for all devices takes place at the buffer/absorber interface, a more significant tunnelling of the charge carriers is obtained for those devices with a CdS layer made at 80 °C, especially by using recipe 2. The lower V_{oc} for those devices is related to the higher defect concentration in the space charge region. This could be due to the higher diffusion of Cu into the buffer layer after the CBD at 80 °C.

Increased efficiency of the devices is possible after their extended storage in air. The enhanced J_{sc} for this case can be explained by diffusion of Cd into the absorber and/or by the passivation of the absorber GBs because of the diffusion of S along GBs. Further investigations are necessary to study the change of the CdS/CGS interface properties.

Acknowledgments

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References

[1] Nishiwaki S, Siebentritt S, Walk P and Lux-Steiner M Ch 2003 *Prog. Photovolt., Res. Appl.* **11** 243
[2] Saad M, Riazi H, Bucger E and Lux-Steiner M Ch 1996 *Appl. Phys.* A **62** 181
[3] Young D L, Keane J, Duda A, AbuShama J A, Perkins C I, Romero M and Noufi R 2003 *Prog. Photovolt., Res. Appl.* **11** 535
[4] Rusu M, Doka S, Kaufmann C A, Grigorieva N, Schedel-Niedrig Th and Lux-Steiner M Ch 2005 *Thin Solid Films* **480/481** 341
[5] Nishiwaki S, Dziedzina M, Schuler S, Siebentritt S, Bär M, Rumberg A, Rusu M, Klenk R and Lux-Steiner M Ch 2003 *Proc. 3rd Conf. on World Photovoltaic Solar Energy Conversion (Osaka)*
[6] Contreras M A, Ramanathan K, AbuShama J, Hasoon F, Young D L, Egaas B and Noufi R 2005 *Prog. Photovolt., Res. Appl.* **13** 209
[7] Klenk R 2001 *Thin Solid Films* **387** 135
[8] Contreras M A, Wiesner H, Tuttle J, Ramanathan K and Noufi R 1997 *Solar Energy Mater. Solar Cells* **49** 239
[9] Nadenau V, Hariskos D and Schock H W 1997 *Proc. 14th Conf. on European Photovoltaic Solar Energy (Barcelona, 30 June–4 July 1997)* ed H A Ossenbrick, P Helm and H Ehmann (Bedford: H S Stephens & Ass) p 1250
[10] Nishiwaki S, Giersig M, Schuler S, Dziedzina M, Siebentritt S and Lux-Steiner M Ch 2001 *Proc. 17th Conf. European Photovoltaic Solar Energy (Munich)* p 1147
[11] Caballero R, Siebentritt S, Sakurai K, Kaufmann C A and Lux-Steiner M Ch 2006 *Proc. IEEE 4th Conf. on World Photovoltaic Energy Conversion (Waikoloa)*
[12] Sakurai K, Hunger R, Scheer R, Kaufmann C A, Yamada A, Baba T, Kimura Y, Matsubara K, Fons P, Nakanishi H and Niki S 2004 *Prog. Photovolt., Res. Appl.* **12** 219

[13] Kaufmann C A, Neisser A, Klenk R and Scheer R 2005 *Thin Solid Films* **480/481** 515
[14] Kohara N, Negami T, Nishitani M and Wada T 1995 *Japan. J. Appl. Phys.* **34** L1141
[15] Nadenau V, Hariskos D, Schock H W, Krejci M, Haug F J, Tiwari A N, Zogg H and Kostorz G 1999 *J. Appl. Phys.* **85** 534
[16] Rusu M, Rumberg A, Schuler S, Nishiwaki S, Würz R, Babu S M, Dziedzina M, Kelch C, Siebentritt S, Klenk R, Schedel-Niedrig Th and Lux-Steiner M Ch 2003 *J. Phys. Chem. Solids* **64** 1849
[17] Caballero R, Siebentritt S, Sakurai K, Kaufmann C A, Schock H W and Lux-Steiner M Ch 2007 *Thin Solid Films* **515** 5862
[18] Dowsett M G 2003 *Appl. Surf. Sci.* **203/204** 5
[19] Nadenau V, Braunger D, Hariskos D and Schock H W 1998 *Inst. Phys. Conf. Ser.* **152** 955
[20] Siebentritt S 2002 *Thin Solid Films* **403/404** 1
[21] Nadenau V, Rau U, Jasenek A and Schock H W 2000 *J. Appl. Phys.* **87** 584
[22] Niemegeers A, Bugelman M, Herberholz R, Rau U, Hariskos D and Schock H W 1998 *Prog. Photovolt., Res. Appl.* **6** 407
[23] Heath J T, Cohen J D and Shafarman W N 2004 *J. Appl. Phys.* **95** 1000
[24] Ortega-Borges R and Lincot D 1993 *J. Electrochem. Soc.* **140** 3466
[25] Ramanathan K, Noufi R, Granata J, Webb J and Keane J 1998 *Sol. Energy Mater. Sol. Cells* **55** 15
[26] Rusu M, Glatzel Th, Neisser A, Kaufmann C A, Sadewasser S and Lux-Steiner M Ch 2006 *Appl. Phys. Lett.* **88** 143510